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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/663,025

09/15/2003

Jia-Fam Wong

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12/29/2005

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EXAMINER

GEBREMARIAM, SAMUEL A

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/663,025

Applicant(s)

WONG, JIA-FAM

Examiner

Samuel A. Gebremariam

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 18-20 and 26-36 is/are pending in the application.
- 4a) Of the above claim(s) 18-20 and 26-28 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 29-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claims 30 and 34 recite the limitation "during (wherein) the etching rate" in line 1.

There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 30 and 34 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The structural relationship between the etching rates as recited in claims 30 and 34 and the claimed device is not clear.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 29-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Sah, US patent No. 6,218,221.

Regarding claim 29, Sah teaches (fig. 8A) a thin film transistor (TFT), comprising: a gate electrode (42) with an island shape formed on a substrate (40); an insulating

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layer (44) covering the gate electrode; a semiconductor layer (46) with an island shape formed on the insulating layer (44), and positioned directly above the gate electrode; a source doped silicon layer (46a) and a drain doped silicon layer (46a) formed on the semiconductor layer (46), a channel (region between the two 46a's) being defined between the source doped silicon layer and the drain doped silicon layer to expose the semiconductor layer therein (refer to fig. 8a); first and second sacrifice layers (48a) with island shapes respectively formed on the source doped silicon layer and drain doped silicon layer (refer to fig. 8a), the first and the second sacrifice layers being spaced apart by the channel and further spaced from the insulating layer (portion of 48a is spaced from the insulating layer 44, refer to fig. 8a); a source electrode (48b) formed above the first sacrifice layer, and the source doped silicon layer (46a); and a drain electrode (48b) formed above the second sacrifice layer on the right hand side (48a) and the drain doped silicon layer (46a).

Regarding claims 30-31, Sah teaches the entire claimed structure of claim 29 above including a passivation layer (52) covering the source electrode (48b), the drain electrode (48b), and the channel.

The limitation of "during the etching process, the etching rate of the first and the second sacrifice layers is RIS, the etching rate and the thickness of the drain doped silicon and the source doped silicon layers are Rn and Tn, and the etching rate and the thickness of the semiconductor layer are Ra and Ta, and the thickness of the first and the second sacrifice layers TIS meets the equation of $(TIS/RIS + Tn/Rn) \leq (Tn/K + Ta/Ra)$ " as recited in claims 30 and 34 is considered a product-by-process claim.

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"[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

The limitation of "the TFT is used in an in-plane-switch (IPS) type LCD" is not given patentable weight because a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Furthermore the structure of Sah can be used as in an in-plane-switch (IPS) type LCD.

Regarding claim 32, Sah teaches the entire claimed structure of claim 29 above including a passivation layer (52) covering the TFT on the substrate (40), and having a hole (56) above the drain electrode (48b); and a transparent conductive layer (54) formed above the drain electrode (48b) and electrically connected to the drain electrode via the hole (refer to fig. 8A).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sah in view of Yang, US patent No. 5,429,962.

Regarding claim 33, Sah teaches (fig. 8a) a thin film transistor (TFT), comprising: a gate electrode (42) with an island shape (refer to fig. 8a) formed on a substrate (40); an insulating layer (44) covering the gate electrode (42); a semiconductor layer (46) with an island shape formed on the insulating layer (44), and positioned above the gate electrode (42, fig. 8a); first and second sacrifice layers (46a on both side of the structure in fig. 8a) with island shapes formed over and in direct contact with the semiconductor layer (46), and a channel being defined between the first and second sacrifice layers (region between 46a's) so as to expose the semiconductor layer (46).

Sah does not teach a source doped silicon layer and a drain doped silicon layer formed above the first sacrifice layer, second sacrifice layer, and the semiconductor layer, the source doped silicon layer and the drain doped silicon layer being spaced apart by the channel; and a source electrode and a drain electrode respectively formed on the source doped silicon layer and the drain doped silicon layer.

Yang teaches (fig. 21, col. 4, lines 8-17) the use of source/drain electrode stack that is formed of a polysilicon layer (11) and a metal layer (12) that are spaced apart by

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the channel region and a source electrode and a drain electrode respectively formed on the source doped silicon region (6a) and the drain doped silicon region (6b).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the source/drain stack taught by Yang in the structure of Sah in order to control and reducing contact resistance (col. 2, lines 45-53). Therefore the combined structure of Sah and Yang would have a source doped silicon layer (polysilicon is doped silicon layer, 11a) and a drain doped silicon layer (polysilicon is doped silicon layer, 11b) formed above the first sacrifice layer (46a on the left hand side), second sacrifice layer (46a on the right hand side), and the semiconductor layer (46), the source doped silicon layer and the drain doped silicon layer being spaced apart by the channel.

Regarding claims 34-35, Sah teaches the substantially entire claimed structure of claim 33 above including a passivation layer (52) covering the source electrode (48b), the drain electrode (48b), and the channel.

The limitation of "during the etching process, the etching rate of the first and the second sacrifice layers is RIS, the etching rate and the thickness of the drain doped silicon and the source doped silicon layers are Rn and Tn, and the etching rate and the thickness of the semiconductor layer are Ra and Ta, and the thickness of the first and the second sacrifice layers TIS meets the equation of $(TIS/RIS + Tn/Rn) \leq (Tn/K + Ta/Ra)$ " as recited in claims 30 and 34 is considered a product-by-process claim. "[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a

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product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.” *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

The limitation of “the TFT is used in an in-plane-switch (IPS) type LCD” is not given patentable weight because a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Furthermore the structure of Sah can be used as in an in-plane-switch (IPS) type LCD.

Regarding claim 36, Sah teaches substantially the entire claimed structure of claim 29 above including a passivation layer (52) covering the TFT on the substrate (40), and having a hole (56) above the drain electrode (48b); and a transparent conductive layer (54) formed above the drain electrode (48b) and electrically connected to the drain electrode via the hole (refer to fig. 8A).

Response to Arguments

7. Applicant's arguments filed 9/30/2005 have been fully considered but they are not persuasive. With regards to claims 29-32 applicant argues that Sah does not

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disclose “the first and the second sacrifice layers further spaced from with the insulating layer” because layer 48a contacts layer 44.

Although the lower portion of layer 48a is contacting layer 44, the top portion of layer 48a is spaced from the insulating layer 44 as claimed. Note the broad recitation of the limitation “the first and second sacrifice layers spaced from the insulating layer” does not preclude portions of the first and second sacrifice layers from contacting the insulating layer.

With regards to claim 33-36 applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

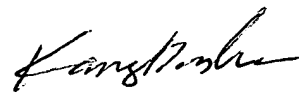
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
December 20, 2005


DONGHEE KANG
PRIMARY EXAMINER